CLAIMS

What is claimed is:

1. A method to manage power in a system, the method comprising:

monitoring transactions over an interconnect coupling a chipset device and a peripheral device in the system, the transactions being transmitted between the peripheral device and the chipset device according to a flow control protocol that allows the chipset device to keep track of the transactions; and

causing a processor in the system to exit from a power state if a plurality of coherent transactions pending in a buffer of the chipset device exceeds a first threshold.

2. The method of claim 1, further comprising:

determining whether a predetermined period of time has passed if the plurality of coherent transactions pending in the buffer does not exceed the first threshold; and

causing the processor to exit from the power state if the predetermined period of time has passed.

3. The method of claim 1, further comprising:

in response to a request from the processor to enter into the power state,

de-asserting an indicator within a message packet to allow the processor to enter into the power state if a plurality of incoherent transactions pending in the buffer of the chipset device exceeds a second threshold.

4. The method of claim 3, further comprising:

asserting the indicator within the message packet to prevent the processor from entering the power state if the plurality of incoherent transactions pending in the buffer of the chipset device exceeds the second threshold.

5. The method of claim 3, further comprising:

determining whether a second predetermined period of time has passed if the plurality of incoherent transactions pending in the buffer of the chipset device is below the second threshold; and

deasserting the indicator within the message packet to allow the processor to enter the power state if the second predetermined period of time has passed.

6. The method of claim 3, wherein the first threshold is substantially equal to the second threshold.

7. The method of claim 3, wherein the first threshold is lower than the second threshold.

8. The method of claim 3, wherein the first threshold is higher than the second threshold.

9. The method of claim 1, wherein the flow control protocol is Peripheral Component Interconnect (PCI) Express.

10. The method of claim 1, wherein the chipset device comprises a memory controller.

11. The method of claim 1, wherein the chipset device comprises an input/output controller.

12. An apparatus in a computing system, the apparatus comprising:

power management circuitry to monitor transactions over an interconnect coupling a root complex device and a peripheral device in the computing system, the transactions being transmitted between the peripheral device and the root complex device according to a flow control protocol to allow the root complex device to keep track of the transactions transmitted; and

a digital media interface coupled to the root complex device to send a first message packet to the root complex device to cause a processor in the computing system to exit from a power state if a plurality of coherent transactions pending in a buffer of the root complex device exceeds a first threshold.

13. The apparatus of claim 12, wherein in response to a request from the processor to enter into the power state, the power management circuitry de-asserts an indicator within a second message packet to allow the processor to enter into the power state if a plurality of incoherent transactions pending in the buffer of the root complex device exceeds a second threshold.

14. The apparatus of claim 13, wherein in response to the request from the processor, the power management circuitry asserts the indicator within the second message packet to prevent the processor from entering the power state if the plurality of incoherent transactions pending in the buffer of the root complex device is below the second threshold.

15. The apparatus of claim 14, further comprising a timer, wherein the power management circuitry asserts the indicator within the second message packet to prevent the processor from entering the power state if the timer has expired.

16. The apparatus of claim 14, wherein the first threshold is substantially equal to the second threshold.

17. The apparatus of claim 12, wherein the flow control protocol is Peripheral Component Interconnect (PCI) Express.

18. A semiconductor chip in a computing system, the semiconductor chip comprising:

a memory controller coupled to a peripheral device in the computing system;

power management circuitry coupled to the memory controller to monitor transactions between the peripheral device and the memory controller; and

an input/output controller residing on a common substrate with the memory controller to allow a processor in the computing system to enter into the power state in

response to a request from the processor to enter into a power state if a plurality of incoherent transactions pending in a buffer of the memory controller exceeds an entry threshold and to prevent the processor from entering into the power state if the plurality of incoherent transactions is below the entry threshold.

19. The semiconductor chip of claim 18, wherein the input/output controller causes the processor to exit from the power state if a plurality of coherent transactions pending in the buffer of the memory controller exceeds an exit threshold.

20. The semiconductor chip of claim 19, wherein the entry threshold is substantially equal to the exit threshold.

21. The semiconductor chip of claim 19, wherein the entry and exit thresholds are adaptively modifiable.

22. The semiconductor chip of claim 18, wherein the peripheral device is coupled to the memory controller via a Peripheral Component Interconnect (PCI) Express interconnect.

23. The semiconductor chip of claim 18, wherein the peripheral device is coupled to the memory controller via a bus.

24. A system comprising:

a processor;

a memory controller coupled to the processor;

a graphics chip;

an interconnect coupling the graphics chip to the memory controller;

an input/output controller, coupled to the memory controller, comprising

power management circuitry to monitor transactions over the interconnect, the transactions being transmitted between the graphics chip and the memory controller according to a flow control protocol; and

a digital media interface coupled to the memory controller to send a first message packet to the memory controller to cause the processor to exit from a power state if a plurality of coherent transactions pending in a buffer of the memory controller exceeds a first threshold.

25. The system of claim 24, wherein the power management circuitry de-asserts an indicator within the second message packet in response to a request from the processor to enter into the power state to allow the processor to enter into the power state if a plurality of incoherent transactions pending in the buffer of the memory controller exceeds a second threshold.

26. The system of claim 25, wherein the power management circuitry asserts the indicator within the second message packet in response to the request from the processor to prevent the processor from entering the power state if the plurality of incoherent

transactions pending in the buffer of the memory controller is below the second threshold.

27. The system of claim 26, wherein the first threshold is substantially equal to the second threshold.

28. The system of claim 24, wherein the flow control protocol is Peripheral Component Interconnect (PCI) Express.